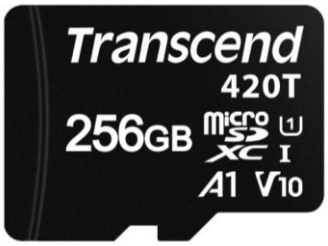
USD420T microSD card

Description

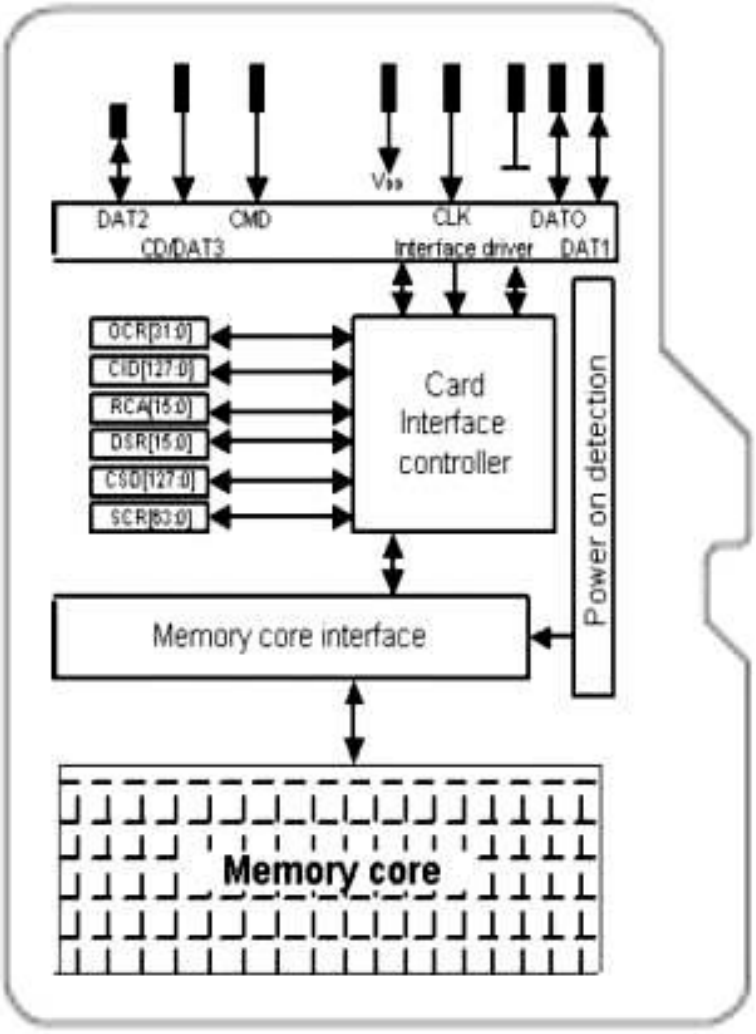
Transcend industrial-grade SD cards offer greater design flexibility and cost savings. Despite their compact size, the SD cards have excellent temperature flexibility from -25°C to 85°C. The cards are manufactured with high-quality controller and 3D NAND flash chips, providing excellent high endurance and performance that help to bring the quality and reliability advantages of industrial memory cards devices.

Features

- Transcend's 3D TLC NAND flash technology
- Operating Temperature: -25 ~ 85°C
- Compatible with SD Specification Ver. 5.1
- UHS-I with Video Speed Class V10
- Application Performance Class1 (A1)
- Early move and Read Retry
- Built-in ECC and Wear leveling
- RoHS compliant product.
- Support ESD IEC 61000-4-2

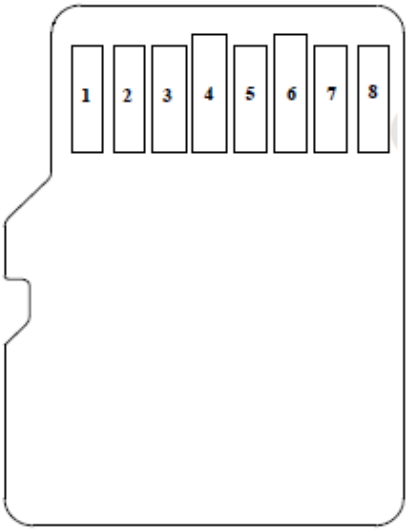


Architecture



Pin Definition

Pin No.	SD Mode		SPI Mode	
	Name	Description	Name	Description
1	DAT2	Data Line [Bit2]	RSV	Reserved
2	CD/DAT3	Card Detect / Data Line [Bit3]	CS	Chip Select
3	CMD	Command / Response	DI	Data In
4	V_{DD}	Supply voltage	V_{DD}	Supply voltage
5	CLK	Clock	SCLK	Clock
6	V_{SS}	Supply voltage ground	V_{SS}	Supply voltage ground
7	DAT0	Data Line [Bit0]	DO	Data out
8	DAT1	Data Line [Bit1]	RSV	Reserved



Specifications

Physical Specification		
Form Factor		microSD
SD specification		SD5.1 (32GB and larger capacity),SD3.01 (16GB)
Flash		3D TLC NAND flash
Dimensions (mm)	**Length**	11.00 ± 0.1
	Width	15.00 ± 0.1
	Height	0.7 ± 0.1

Data Transfer Specification				
Model P/N	**SD Type**	**Interface***	**Speed Class**	**Application Performance Class**
TS16GUSD420T	SDHC	UHS-I SDR104	C10/U1	N/A
TS32GUSD420T	SDHC	UHS-I SDR104	V10/U1	A1
TS64GUSD420T	SDHC	UHS-I SDR104	V10/U1	A1
TS128GUSD420T	SDHC	UHS-I SDR104	V10/U1	A1
TS256GUSD420T	SDHC	UHS-I SDR104	V10/U1	A1

Note: All parameters are determined by Testmetrix VTE4100
*Only shows the fastest transferring bus mode

Performance				
Model P/N	**Sequential Read***	**Sequential Write***	**Random Read IOPS**** (4KB QD32)	**Random Write IOPS**** (4KB QD32)
TS16GUSD420T	90	25	1900	200
TS32GUSD420T	95	25	3000	800
TS64GUSD420T	95	25	3000	800
TS128GUSD420T	95	40	3000	900
TS256GUSD420T	95	40	3000	900

Note: Maximum transfer speed recorded

* 25 ℃ , 4GB DRAM, Windows® 7 with Transcend RDF5, benchmark utility Crystal Disk Mark , copied file 1000MB, unit MB/s

** 25 ℃ , 4GB DRAM, Windows® 7 with Transcend RDF5, benchmark IO Meter 2008 , copied 4GB size ,unit IOPS

Endurance		
TeraBytes Written (T.B.)	TS16GUSD420T	13
	TS32GUSD420T	80
	TS64GUSD420T	160
	TS128GUSD420T	320
	TS256GUSD420T	640

*TBW is based on Transcend internal standard to calculate how much data can be written into the drive.
*1 TeraByte=1,000,000,000 byte

Bus Mode/ Power Consumption		
		Value(Max.)
Default Mode (25MHz)	**Read**	100mA
	Write	100mA
	Idle	0.5mA
High Speed mode (50MHz)	**Read**	200mA
	Write	200mA
	Idle	0.5mA
UHS-I SDR50 mode (100MHz)	**Read**	400mA
	Write	400mA
	Idle	0.5mA
UHS-I DDR50 mode (50MHz)	**Read**	400mA
	Write	400mA
	Idle	0.5mA
UHS-I SDR104 mode (208MHz)	**Read**	800mA
	Write	800mA
	Idle	0.5mA

Note: Power consumption is referred to Section 6.6.3 of the SDA Physical Layer Specification, Version 5.1

Environmental Specifications	
Operating Temperature	- 25℃ to 85℃
Storage Temperature	- 40℃ to 85℃
Durability	10.000 mating cycles
Drop test	1.5m free fall
Regulator	CE/FCC/BSMI

Product Description

1.Features

1.1 Lock Function

Support for password protected locking and unlocking of SD devices. It uses the LOCK/UNLOCK command(CMD42) which is available in SD command sets.

1.2 Built-in ECC Engine

In event of errors, the combined data allow the recovery of the original data. The number of errors that can be recovered depends on the algorithm used.

1.3 Wear-leveling

This function means the data are no longer tied to a single physical area, which can extend Card's life expectancy.

1.4 Early move

The function provides a mechanism to avoid read disturbance. Built-in ECC is used to detect and correct data bit error. If error bits reaches the default threshold, the data will be moved to another good block to avoid un-correct error in advance.

1.5 Read Retry

The function allows the read voltage to be dynamically adjusted such that read errors are decreased or even eliminated.

2.Bus Topology

The SD Memory Card system defines two alternative communication protocols:SD and SPI. The host system can choose either one of modes. The card detects which mode is request by host when the reset command is received and expects all further communication to be in the same communication mode.

2.1 SD Bus

For more details, refer to Section 3.5.1 of the SDA Physical Layer Specification, Version 5.1

2.2 SPI Bus

For more details, refer to Section 3.5.2 of the SDA Physical Layer Specification, Version 5.1.

3.SD card Register information

3.1 OCR register

The OCR 32-bit operation conditions register stores the VDD voltage profile of the non UHS-II card and VDD1 voltage profile of the UHS-II card. Additionally, this register includes status information bits. One status bit is set if the card power up procedure has been finished. This register includes another status bit indicating the card capacity status after set power up status bit

OCR bit position	OCR Fields Definition
0-3	reserved
4	reserved
5	reserved
6	reserved
7	Reserved for Low Voltage Range
8	reserved
9	reserved
10	reserved
11	reserved
12	reserved
13	reserved
14	reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24	Switching to 1.8V Accepted (S18A)
25-28	reserved
29	UHS-II Card Status
30	Card Capacity Status (CCS)1
31	Card power up status bit (busy)2

1) This bit is valid only when the card power up status bit is set.

2) This bit is set to LOW if the card has not finished the power up routine.

3.2 CID register

The Card Identification (CID) register is 128 bits wide. It contains the card identification information used during the card identification phase. Every individual flash card shall have a unique identification number. The structure of the CID register is defined in the following paragraphs:

Name	Field	Width	CID-slice
Manufacturer ID	MID	8	[127:120]
OEM/Application ID	OID	16	[119:104]
Product name	PNM	40	[103:64]
Product revision	PRV	8	[63:56]
Product serial number	PSN	32	[55:24]
reserved	--	4	[23:20]
Manufacturing date	MDT	12	[19:8]
CRC7 checksum	CRC	7	[7:1]
not used, always '1'	-	1	[0:0]

• MID

An 8-bit binary number that identifies the card manufacturer. The MID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

• OID

A 2-character ASCII string that identifies the card OEM and/or the card contents (when used as a distribution media either on ROM or FLASH cards). The OID number is controlled, defined, and allocated to a SD Memory Card manufacturer by the SD-3C, LLC. This procedure is established to ensure uniqueness of the CID register.

•PNM

The product name is a string, 5 ASCII characters long.
PNM can be customized by Transcend

• PRV

The product revision is composed of two Binary Coded Decimal (BCD) digits, four bits each, representing an

"n.m" revision number. The "n" is the most significant nibble and "m" is the least significant nibble.
As an example, the PRV binary value field for product revision "6.2" will be: 0110 0010
PRV can be customized by Transcend

• PSN
The Serial Number is 32 bits of binary number.
PSN Number can be customized by Transcend

• MDT
The manufacturing date composed of two hexadecimal digits, one is 8 bit representing the year(y) and the other is four bits representing the month(m).
The "m" field [11:8] is the month code. 1 = January.
The "y" field [19:12] is the year code. 0 = 2000.
As an example, the binary value of the Date field for production date "April 2001" will be: 00000001 0100.
MDT can be customized by Transcend

• CRC
CRC7 checksum (7 bits).

3.3 CSD register

The following sections describe the CSD fields and the relevant data types for the standard and High Capacity SD Memory Card. CSD Version 1.0 is applied Capacity SD Memory Card and CSD Version is applied to 2.0 is applied to only the High Capacity SD Memory Card. The field name in parenthesis is set to fixed value and indicates that the host is not necessary to refer these fields. The fixed values enables host, which refers to these fields, to keep compatibility to CSD Version 1.0. The Cell Type field is coded as follows: R = readable, W(1) = writable once, W = multiple writable.

3.3.1 CSD Register Structure

CSD_STRUCTURE	CSD Structure version	Card capacity
0	CSD Version1.0	Standard Capacity
1	CSD Version2.0	High Capacity and Extended Capacity
2-3	reserved	

3.3.2 CSD Register Structure (CSD Version 1.0)

Name	Field	Width	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	R	[127:126]
reserved	-	6	R	[125:120]
data read access-time-1	TAAC	8	R	[119:112]
data read access-time-2 in CLK cycles (NSAC*100)	NSAC	8	R	[111:104]
max. data transfer rate	TRAN_SPEED	8	R	[103:96]
card command classes	CCC	12	R	[95:84]
max. read data block length	READ_BL_LEN	4	R	[83:80]
partial blocks for read allowed	READ_BL_PARTIAL	1	R	[79:79]
write block misalignment	WRITE_BLK_MISALIGN	1	R	[78:78]
read block misalignment	READ_BLK_MISALIGN	1	R	[77:77]
DSR implemented	DSR_IMP	1	R	[76:76]
reserved	-	2	R	[75:74]
device size	C_SIZE	12	R	[73:62]
max. read current @VDD min	VDD_R_CURR_MIN	3	R	[61:59]
max. read current @VDD max	VDD_R_CURR_MAX	3	R	[58:56]
max. write current @VDD min	VDD_W_CURR_MIN	3	R	[55:53]
max. write current @VDD max	VDD_W_CURR_MAX	3	R	[52:50]

3.3.3 CSD Register (CSD Version 2.0)

Name	Field	Width	Value	Cell Type	CSD-slice
CSD structure	CSD_STRUCTURE	2	01b	R	[127:126]
reserved	-	6	00 0000b	R	[125:120]
data read access-time	(TAAC)	8	0Eh	R	[119:112]
data read access-time in CLK cycles (NSAC*100)	(NSAC)	8	00h	R	[111:104]
max. data transfer rate	(TRAN_SPEED)	8	32h or 5Ah	R	[103:96]
card command classes	CCC	12	01x110110101b	R	[95:84]
max. read data block length	(READ_BL_LEN)	4	9	R	[83:80]
partial blocks for read allowed	(READ_BL_PARTIAL)	1	0	R	[79:79]
write block misalignment	(WRITE_BLK_MISALIGN)	1	0	R	[78:78]
read block misalignment	(READ_BLK_MISALIGN)	1	0	R	[77:77]
DSR implemented	DSR_IMP	1	x	R	[76:76]
reserved	-	6	00 0000b	R	[75:70]
device size	C_SIZE	22	00 xxxxh	R	[69:48]
reserved	-	1	0	R	[47:47]
erase single block enable	(ERASE_BLK_EN)	1	1	R	[46:46]
erase sector size	(SECTOR_SIZE)	7	7Fh	R	[45:39]
write protect group size	(WP_GRP_SIZE)	7	0000000b	R	[38:32]
write protect group enable	(WP_GRP_ENABLE)	1	0	R	[31:31]
reserved		2	00b	R	[30:29]
write speed factor	(R2W_FACTOR)	3	010b	R	[28:26]
max. write data block length	(WRITE_BL_LEN)	4	9	R	[25:22]
partial blocks for write allowed	(WRITE_BL_PARTIAL)	1	0	R	[21:21]
reserved	-	5	00000b	R	[20:16]
File format group	(FILE_FORMAT_GRP)	1	0	R	[15:15]
copy flag (OTP)	COPY	1	x	R/W(1)	[14:14]
permanent write protection	PERM_WRITE_PROTECT	1	x	R/W(1)	[13:13]
temporary write protection	TMP_WRITE_PROTECT	1	x	R/W	[12:12]
File format	(FILE_FORMAT)	2	00b	R	[11:10]
reserved	-	2	00b	R	[9:8]
CRC	CRC	7	xxxxxxxb	R/W	[7:1]
not used, always'1'	-	1	1	-	[0:0]

3.4 RCA register

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA

3.5 SCR register

In addition to the CSD register, there is another configuration register named SD CARD configuration Register, SCR provide information on the SD memory card's special feature that were configured into the given card.

The size of SCR register is 64 bits. This register shall be set in the factory by Transcend. The following table describes the SCR register content

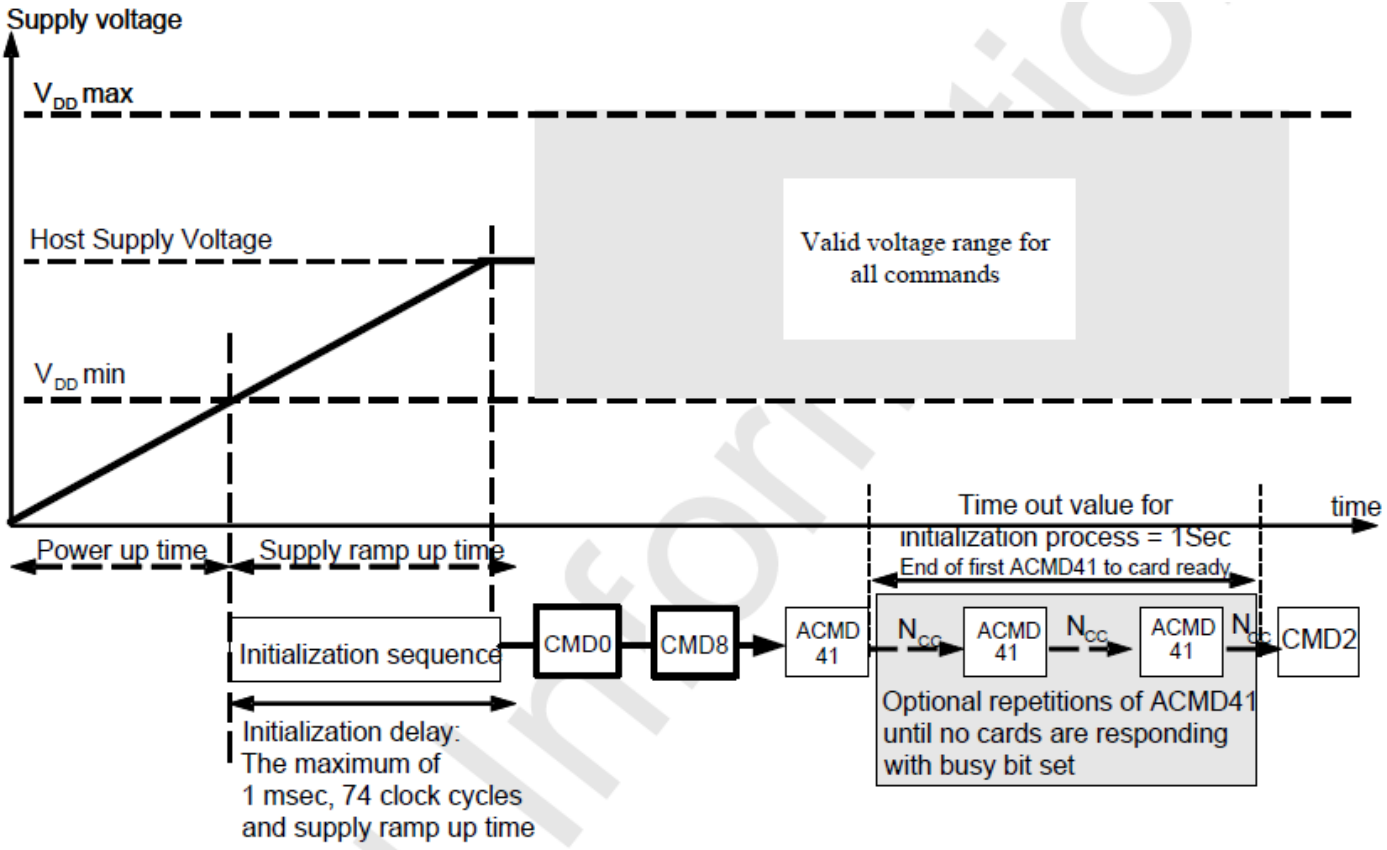
Description	Field	Width	Cell Type	SCR Slice
SCR Structure	SCR_STRUCTURE	4	R	[63:60]
SD Memory Card - Spec. Version	SD_SPEC	4	R	[59:56]
data_status_after erases	DATA_STAT_AFTER_ERASE	1	R	[55:55]
CPRM Security Support	SD_SECURITY	3	R	[54:52]
DAT Bus widths supported	SD_BUS_WIDTHS	4	R	[51:48]
Spec. Version 3.00 or higher	SD_SPEC3	1	R	[47]
Extended Security Support	EX_SECURITY	4	R	[46:43]
Spec. Version 4.00 or higher	SD_SPEC4	1	R	[42]
Spec. Version 5.00 or higher	SD_SPECX	4	R	[41:38]
Reserved		2	R	[37:36]
Command Support bits	CMD_SUPPORT	4	R	[35:32]
reserved for manufacturer usage	-	32	R	[31:0]

The writable 16-bit relative card address register carries the card address that is published by the card during the card identification. This address is used for the addressed host-card communication after the card identification procedure. The default value of the RCA

4.0 Power Scheme

4.1.1 Power Up Time of Card

A card shall be ready to accept the first command within 1ms from detecting VDD min. The host may use up to 74 clocks for preparation before receiving the first command.



Power up time is defined as voltage rising time from 0 volt to VDD min and depends on application parameters such as the maximum number of SD Cards, the bus length and the characteristic of the power supply unit.

Supply ramp up time provides the time that the power is built up to the operating level (Host Supply Voltage) and the time to wait until the SD card can accept the first command,

The host shall supply power to the card so that the voltage is reached to Vdd_min within 250ms and start to supply at least 74 SD clocks to the SD card with keeping CMD line to high. In case of SPI mode, CS shall be held to high during 74 clock cycles.

After power up (including hot insertion, i.e. inserting a card when the bus is operating) the SD Card enters the *idle state*. In case of SD host, CMD0 is not necessary. In case of SPI host, CMD0 shall be the first command to

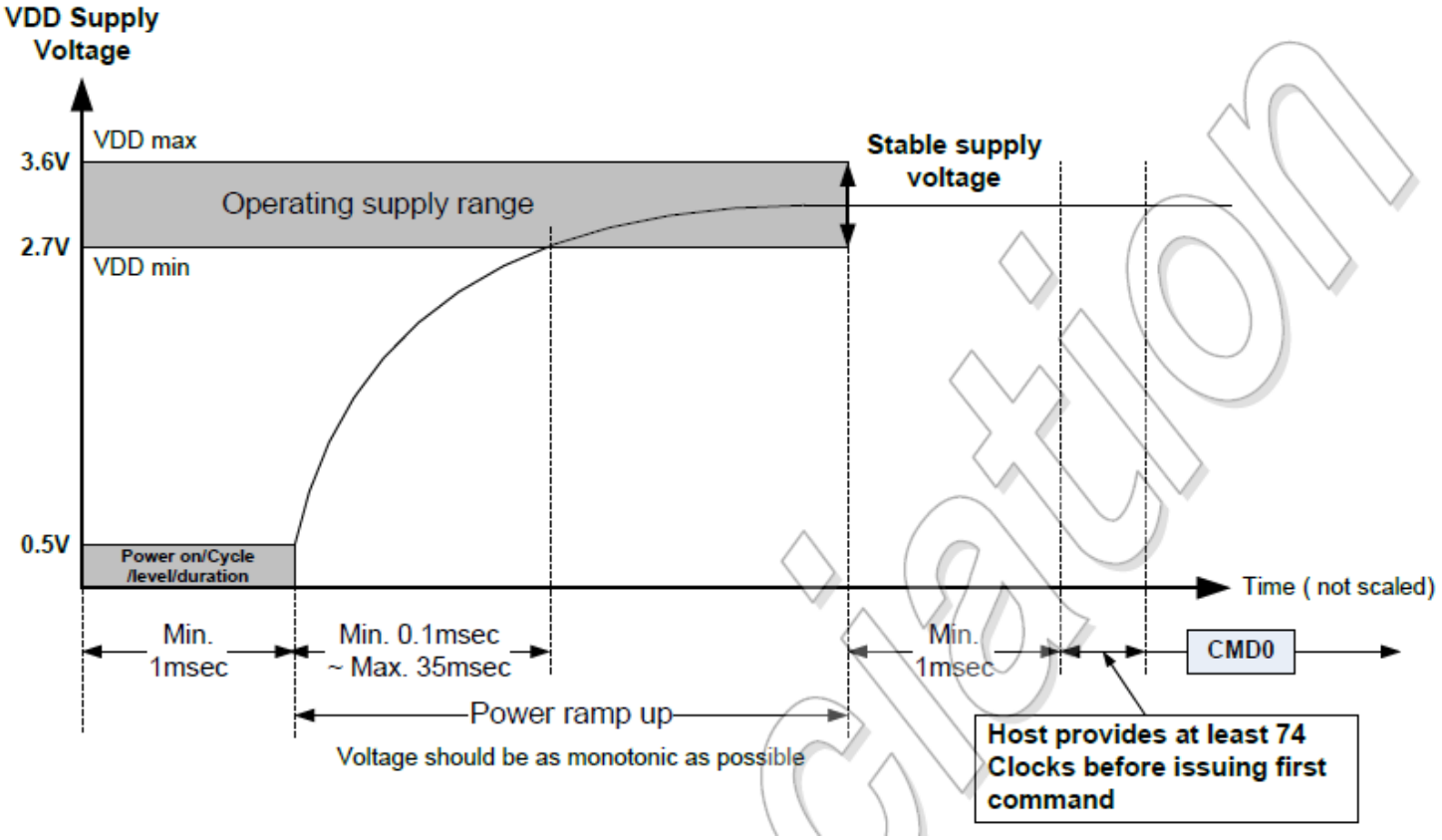
send the card to SPI mode.

CMD8 is newly added in the Physical Layer Specification Version 2.00 to support multiple voltage ranges and used to check whether the card supports supplied voltage. The version 2.00 or later host shall issue CMD8 and verify voltage before card initialization. The host that does not support CMD8 shall supply high voltage range.

ACMD41 is a synchronization command used to negotiate the operation voltage range and to poll the cards until they are out of their power-up sequence. In case the host system connects multiple cards,the host shall check that all cards satisfy the supplied voltage. Otherwise, the host should select one
of the cards and initialize

4.1.2 Power Up Time of Host

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up



4.1.3 Power On or Power Cycle

Followings are requirements for Power on and Power cycle to assure a reliable SD Card hard reset.

(1) Voltage level shall be below 0.5V

(2) Duration shall be at least 1ms.

4.1.4 Power Supply Ramp Up

The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VDD(min.) and VDD(max.) and host can supply SDCLK.

Followings are recommendation of Power ramp up:

(1) Voltage of power ramp up should be monotonic as much as possible.

(2) The minimum ramp up time should be 0.1ms.

(3) The maximum ramp up time should be 35ms for 2.7-3.6V power supply.

(4) Host shall wait until VDD is stable.

(5) After 1ms VDD stable time, host provides at least 74 clocks before issuing the first command.

4.1.5 Power Down and Power Cycle

When the host shuts down the power, the card VDD shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing cards that are already in *Inactive State.* To create a power cycle the host shall follow the power down description before power up the card (i.e. the card VDD shall be once lowered to less than 0.5Volt for a minimum period of 1ms).

The above technical information is based on industry standard data and has been tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes to the specifications at any time without prior notice.

Order information

Capacity	Transcend Part Number
16GB	TS16GUSD420T
32GB	TS32GUSD420T
64GB	TS64GUSD420T
128GB	TS128GUSD420T
256GB	TS256GUSD420T

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Revision History

Version	Date	Note
0.1	2019/08/15	The 1st W edition
1.0	2019/10/22	Update performance
1.1	2020/01/14	Add 256GB
1.2	2020/02/06	Correct TBW (TS256GUSD420T)
1.3	2020/03/17	Add 16GB SKU
1.4	2020/04/28	Add U1 in data transfer specification for TS16GUSD420T
1.5	2020/05/08	Add feature / Specification